Notice of References Cited	Application/Control No. 09/893,527	Applicant(s)/Patent Under Reexamination WIMER, SHMUEL	
	Examiner Dwin M Craig	Art Unit 2123	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-6,393,601 B1	05-2002	Tanaka et al.	716/2
*	B	US-6,006,024 A	12-1999	Guruswamy et al.	716/12
*	C	US-5,987,086 A	11-1999	Raman et al.	716/1
*	D	US-5,984,510 A	11-1999	Guruswamy et al.	716/2
*	E	US-6,209,123 B1	03-2001	Maziasz et al.	716/14
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	John Valainis, Sinan Kaptanoglu, Erwin Liu, Robert Suaya, "Two-Dimensional IC Layout Compaction Based on Topological Design Rule Checking" IEEE 1990, pages 260-275.
	V	Nikolaos G. Bourbakis, Mohammad Mortazavi, "An Efficient Building Block Layout Methodology For Compact Placement" IEEE 1995, pages 118-123.
	W	Lack A. Feldman, Israel A. Wagner, Shmuel Wimer, "An Efficient Algorithm for Some Multirow Layout Problems", IEEE 1993, pages 1178-1185.
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.